

GLOBAL SEMICONDUCTOR PACKAGING MATERIALS OUTLOOK



Produced by TechSearch International, Inc. and SEMI

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TechSearch International, Inc. and SEMI® have cooperated in the development of the ninth edition of the Global Semiconductor Packaging Materials Outlook, a comprehensive market research study on the semiconductor packaging materials market. For this edition of the report, TECHCET LLC provided SEMI coverage of the leadframe, bonding wire, encapsulant materials, and die attach markets.

Interviews were conducted with more than 100 semiconductor manufacturers, packaging subcontractors, fabless semiconductor companies, and packaging material suppliers to gather information for this report. The following semiconductor packaging materials segments are covered: substrates, leadframes, bonding wire, encapsulants, underfill materials, die attach, solder balls, wafer level package dielectrics, and wafer level plating chemicals. The information contained in this report was developed by TechSearch International and/or SEMI and its partner TECHCET LLC.

Smartphone unit growth remains a key driver of semiconductor and packaging technology. Besides mobility, major growth drivers in the electronics and semiconductor industries are connectivity, big data processing/high performance computing (HPC), data storage/advanced memory, and automotive electronics. HPC, big data analytics, storage, and communications will drive high-value packaging. Such packaging technologies include silicon interposers to deliver heterogeneous integration and High-Bandwidth Memory (HBM). Alternatives based on RDL substrates are being developed to lower costs while providing the higher degree of integration required for emerging packaging solutions.

5G, heterogeneous integration, and multi-die solutions are other key drivers for packaging development going forward, and will require advancements in materials to deliver performance and reliability. For panel Fan Out (FO), dielectric material selection and dispense methods will be important to successfully ramp in high volume.

Advancements and changes continue in the semiconductor packaging materials market, and over the next several years some areas of opportunity include:

- Continuing improvements in substrate design help to compensate for the CTE mismatch between the die and the substrate
- FC-BGA substrate core thickness down to 0.1 mm or 0.2 mm
- Substrates with <5 μm lines and spaces and 30 μm via diameters in the build-up layers.
- Core layers with 20 μm lines and spaces with vias as small as 50 μm and capture pads as small as 110 μm
- Low D_k and D_f laminate materials for 5G mmWave applications
- Embedded bridge chip in the laminate substrate
- Coreless structure based on a modified leadframe technology called a Molded Interconnect Solution/System (MIS)
- QFN package designs for automotive applications
- Cost reductions for QFN power packages, including Cu clip, and Intelligent Power Modules (IPM) leadframe-based packages

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- Softer, reliable copper alloy wire, including new alloying elements, antioxidant alloys, and surface treatments for wire materials improvement
- Silver alloy wire and gold-coated silver wire to provide lower material cost, yet higher reliability wire solutions for automotive applications
- Replacement of multiple aluminum wires with aluminum ribbon for lower parasitics at high frequencies and lower current density, permitting higher current in power applications

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- Mold compounds to provide underfill for copper pillar flip chip
- Need smaller fillers and narrower particle size distribution for better warpage control, especially critical in Fan Out WLP (FO-WLP)
- Thermally enhanced and high-voltage mold compounds for power and automotive devices
- Continue improvement in the stability and refractive index of LED encapsulants
- New underfill resin and filler formulations to address the smaller gaps and fine pitch flip chip and with some stacked-die applications
- Reducing underfill resin bleed-out required with smaller keep-out zone in small, thin packaging
- Die attach materials with no-to-low resin bleed; no-to-low outgassing; and processed within <5 µm placement

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- New low stress die attach materials for sensor and SIP applications
- Thermally conductive die attach materials with thermal conductivity >70 W/K and with a low elastic modulus and a cure temperature of 200°C or less
- WLP dielectrics with low temperature cure (230°C and below)
- Low-stress dielectric materials with low process temperatures for panel FO, and capable to support fine features roadmaps (≤10 µm lines and spaces)
- Dielectrics for higher frequency applications such as 5G, lower dielectric loss (Df) are required
- Advancement in solder ball alloys to improve drop test reliability
- Plastic core with Pb-free plating to achieve a higher standoff and improved mechanical reliability
- Key for plating chemicals is robust bath life, reasonably high deposition rate, wide process windows, and repeatable and controllable feature profiles (flat preferred)
- For RDL plating, high purity Cu is important, and for 5G applications, low surface roughness is required for high frequency
- Specific for TSV plating, void free deposition and low overburden deposition

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In total, the semiconductor packaging materials market covered in this study was \$17.6 billion in 2019 globally, and it is forecasted to be \$20.8 billion in 2024, a 3.4% CAGR. In general, the revenue growth is in-line with semiconductor industry unit growth. Laminate substrates, the largest materials segment, will grow at over a 5% CAGR with demand for SIP and high-performance devices. WLP dielectric will have the highest CAGR, >9%, over the forecast period given the strong growth in this package form factor. The trend towards smaller, thinner packaging will dampen the growth rate of leadframes, die attach, and encapsulant materials.

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The global market for laminate substrates for IC packages is forecasted to experience a compound annual growth rate (CAGR) of 5% from 2019 through 2024 based on square meters of materials processed. Larger package sizes are driving area growth. The growth rate for CSP 8%, including both wire bond and flip chip packages, is the highest of the segments, while wire bond PBGA substrates will decline over the forecast period.

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Overall leadframe shipments are forecasted to grow just over 3% CAGR from 2019 through to 2024, with LFCSP (QFN type) experiencing the strongest unit growth, almost a 7% CAGR. Over the same period, leadframe revenues are forecasted to grow by less than a 1% CAGR.

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Total copper wire is at over 54% share of the bonding wire shipments, while gold wire has declined to under a 32% share. Total wire shipments were over 24 billion meters in 2019 and are forecasted to grow at a 2% CAGR through to 2024.

For encapsulation material revenues, the 2019 to 2024 CAGR will be just under 3% given the growth in smaller, thinner packaging form factors. Revenues were \$2.5 billion in 2019. Japanese suppliers maintain a dominate position in mold compounds, while China suppliers of liquid encapsulation materials for LED continue to gain market share.

The main application for underfill remains flip chip packaging, but as bump pitches shrink limitations of the current capillary UF process and materials demand that alternatives be explored. Molded underfill (MUF) is one approach. Underfill development work is focused materials and processes for void-free materials as gap height and bump pitches are reduced. NCF continues to be used for HBM applications. The total underfill market was \$208 million in 2019 and will grow at a 4.5% CAGR through 2024.

Die attach material revenues reached \$740 million in 2019 and will grow an estimated CAGR of under 4% through to 2024. Sintered materials have been developed for high temperature applications that require lower process temperatures compared to solder die attach. This market was estimated to be in the range of \$9 million to \$10 million in 2019.

Solder ball revenues reached \$236 million in 2019 and will grow by about 3% CAGR through to 2024. The revenue outlook depends on fluctuations in metal pricing, especially silver (Ag), as the most common type of solder is based on tin-silver-copper (SAC). New entrants headquartered in China have emerged.

The WLP dielectrics market reached \$232 million in 2019 and is forecasted to grow over 9% CAGR through 2024. High-density FOWLP will require multiple RDL, while dielectric solutions are being developed for larger panel applications.

The wafer-level plating chemical market was estimated to be \$335 million in 2019 and will grow by over 7% CAGR through 2024. SnAg chemistry for solder bumping remains the largest segment through the forecast period with the highest CAGR.

The forecast 2020 global market size and key trends in each semiconductor packaging materials segment are summarized on the following page.

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2020 GLOBAL MARKET SIZE AND KEY TRENDS IN SEMICONDUCTOR PACKAGING MATERIALS SEGMENTS

Semiconductor Packaging Materials Segment	Estimate for 2020 Global Market Size \$B	Comments
Laminate Substrates	\$7.7	Flip chip packages for servers, network switches, and other high-performance devices are increasing in both body size and unit volumes. Increasing development of substrates with embedded bridge structures. Companies have introduced new film materials with improved surface roughness to support finer line and spaces below 10 μm for substrates.
Leadframes	\$3.0	Consolidation occurring, especially within the Japanese leadframe industry. LFCSP remains the growth segment, with formats for flip chip and automotive growing.
Bonding Wire	\$3.1	Alloy/additive development for low loop height and looping control in thin and multi-die packages. Wire bond to be used in low-density memory consumed in Internet of Things (IoT). Growing capability and market share of Chinese wire suppliers, especially within China.
Encapsulant Materials	\$2.5	Japan suppliers maintain strong share of mold compound market, while China suppliers ramp LED encapsulant materials. Compression molding with smaller filler size for thinner packages. Low D_f and D_k properties high-frequency device applications. Molded underfill has increased for applications such as CSPs.
Underfill Materials	\$0.2	Suppliers continue to develop improved materials for finer pitch and smaller gaps CUF is the largest segment. HBM drives growth for NCF adoption. Two dozen plus suppliers with newer ones from Korea and China.
Die Attach Materials	\$0.74	Stable paste supplier base. Paste development around modified resin systems for low stress. Materials with high thermal conductivity (70 W/K and even >100 W/K) and low elastic modulus.
Solder Balls	\$0.24	Alloying/additives to improve mechanical drop test performance. Plastic core for higher standoff and improved mechanical performance. New suppliers in China.
Wafer Level Package Dielectrics	\$0.23	Shift to FO-WLP from laminate flip. Supply base dominated by Japanese suppliers. New RDL materials formulations with low stress/low modulus properties
Wafer Plating Chemicals	\$0.34	Numerous suppliers globally. Cu pillar is increasingly used for finer pitch and superior electromigration performance for high current density. Plating uniformity across the wafer important for bump/pillar coplanarity and essential for good assembly.

Source: TechSearch International and SEMI/TECHCET June 2020